REMARKS

In response to the Office Action of May 16, 2005, Applicants respectfully request reconsideration. Claims 1-19 were previously pending in this application. Claim 1 has been amended. No new claims have been added. As a result, claims 1-19 are pending for examination with claims 1, 10, and 15 being independent. The application is believed to be in condition for allowance. No new matter has been added.

Summary of Telephone Conference with Examiner

Applicants' representatives appreciate the courtesies extended by Examiner Trinh in granting and conducting the telephone conference of August 16, 2005. The substance of the telephone conference is summarized herein.

Rejections under 35 U.S.C. §112, First Paragraph

The Office Action rejects claim 1 under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement.

As discussed during the telephone conference, the subject matter of the added limitation "the two programming terminals being different from said input/output terminals," is shown in Figures 3, 4A, and 4B and described in the specification on page 8, lines 13-15 and lines 25-28. Specifically, Figures 3-4B and the cited portion of the specification show and describe terminals 11 and 12 (the "input/output terminals") being different from terminals 13 and 14 (the "programming terminals"). In view of this discussion, the Examiner indicated that the added language did not appear to be new matter.

Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §112, first paragraph, is respectfully requested.

Rejections under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claim 1 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

Claim 1 has been amended to clarify that both the input/output terminals and the programming terminals are intended to receive a supply voltage, but the input/output terminals and the programming terminals are distinct.

Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §112, second paragraph, is respectfully requested.

It should be appreciated that the amendment to claim 1 is made solely for the purpose of clarification and is not intended to alter the scope of the claim. Thus, the amendment raises no new issues that would require further search and/or consideration.

Rejections Under 35 U.S.C. §102

The Office Action rejects claims 1, 2, 4, and 6-9 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,418,738 (Abadeer). Applicants respectfully traverse this rejection.

The Office Action asserts that Abadeer teaches resistors connected in a parallel association between two programming terminals T_b and T_d intended to receive a supply voltage V_{dd}. Applicants respectfully disagree.

Abadeer describes a programmable storage element which includes a plurality of first resistors and a switching circuit for coupling the first resistors in series in response to a plurality of first control signals. The switching circuit also couples the first resistors in parallel in response to a plurality of second control signals to permit programming of the first resistors (abstract). The device described by Abadeer in Figure 3 (relied upon in the Office Action) contains four transistors Q_{fa} - Q_{fd} receiving a plurality of *control signals* at control terminals T_a - T_d respectively (Col. 7, lines 8-10). Resistors F_{1A}, F_{1B} and F_{1C} are connected in series between a supply voltage source V_{dd} and an output terminal T (Col. 7, lines 20-22).

Claims 1, 2, 4 and 6-9:

Claim 1 is directed to a resistive element controllable to irreversibly decrease its value, comprising several polysilicon resistors connected in series between two input/output terminals of the resistive element, and an assembly of switches, connected to turn the series connection into a parallel association of said resistors between two programming terminals, the two

programming terminals being different from said input/output terminals, the two programming terminals intended to receive a supply voltage.

Abadeer does not teach or suggest an assembly of switches, connected to turn the series connection into a parallel association of said resistors between two programming terminals, the two programming terminals being different from said input/output terminals, *the two programming terminals intended to receive a supply voltage*, as recited in claim 1. As discussed above, terminals T_b and T_d do not receive a supply voltage, but instead only receive a *control signal*.

In view of the foregoing, claim 1 patentably distinguishes over Abadeer. Thus, the rejection under §102 is improper and should be withdrawn. Claims 2-9 depend from claim 1 and are patentable for at least the same reasons.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 3, 5, and 10-19 under 35 U.S.C. §103(a) as allegedly being unpatentable over Abadeer in view of U.S. Patent No. 5,638,029 (O'Shaughnessy). These rejections are respectfully traversed.

The Office Action asserts Abadeer discloses the invention substantially as claimed but concedes that Abadeer does not explicitly teach that the resistive element comprises MOS transistors with N-channel and P-channel transistors, whereby the number of N-channel transistors is equal to or greater by one than the number of P-channel transistors. However, the Office Action concludes that it would have been obvious to modify the invention of Abadeer with MOS transistors having N-channel and P-channel transistors, whereby the number of N-channel transistors is equal to or greater by one than the number of P-channel transistors, in order to provide a better control of the signal timing in a circuit. Applicants respectfully disagree.

O'Shaughnessy describes a clock overdrive function which facilitates the testing of circuits incorporating timing circuits (abstract). The device in O'Shaughnessy includes a clock overdrive circuit for overdriving a timing signal of a system clock, which includes a RC circuit. (Col. 2, lines 11-12). In Figure 2 (relied upon by the Office Action), a transistor-level schematic diagram of self-calibrating RC oscillator circuit is depicted, which includes 11 P-channel MOS transistors (411, 412, 431, 422, 433, 434, 471, 473, 474, 476, and 477) and 7 N-channel MOS transistors (413, 414, 416, 436, 424, 478, and 479).

The Combination of Abadeer and O'Shaughnessy is Improper:

As discussed during the telephone conference, a *prima facie* case of obviousness requires some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings (MPEP § 2143). O'Shaughnessy does not teach or suggest that the use of a number of P-channel transistors equal to or greater than the number of N-channel transistors improves the control of circuit timing. Further, Applicants respectfully assert that there is nothing in the prior art of record that would have motivated one of ordinary skill in the art to modify the device of Abadeer, based on the teachings of O'Shaughnessy, so that the number of transistors of a P-channel type are equal to or greater than those of N-channel type. Indeed, the Office Action does not point to any teachings in either Abadeer or O'Shaughnessy in support of the alleged motivation to combine the reference teachings.

If the assertion that it would have been obvious to modify the invention of Abadeer with MOS transistors having N-channel and P-channel transistors, whereby the number of N-channel transistors is equal to or greater by one than the number of P-channel transistors is to be maintained, the Examiner is respectfully requested to cite a reference in support of this position, as required under MPEP § 2144.03. Alternatively, if facts within the Examiner's personal knowledge are being relied upon, the Examiner is respectfully requested to file an affidavit establishing those facts pursuant to MPEP § 2144.03.

The Claims Patentably Distinguish over Any Combination of Abadeer and O'Shaughnessy:

Even if one of ordinary skill in the art would have been motivated to combine Abadeer and O'Shaughnessy for the purpose of achieving precise control of circuit timing, which Applicants do not concede, the resulting combination would include the programmable storage element featured in Abadeer with an external self-calibrating RC oscillator circuit as taught by O'Shaughnessy. This resulting combination of Abadeer and O'Shaughnessy would not yield the invention of each of claims 10-19 for the reasons discussed below.

Claims 10-14:

Claim 10 is directed to a resistive element controllable to irreversibly decrease its value, comprising several polysilicon resistors connected in series between two input/output terminals of the resistive element, an assembly of switches, connected to turn the series connection into a parallel association of said resistors between two programming terminals intended to receive a supply voltage, wherein the assembly of switches comprises one more switch than the resistive element comprises resistors, one of the switches connecting one of said input/output terminals to one of said programming terminals, and wherein the assembly of switches further comprises MOS transistors with a number of N-channel transistors greater by one than the number of P-channel transistors.

Claim 10 patentably distinguishes from the combination of Abadeer and O'Shaughnessy for at least two reasons. First, as should be appreciated from the above discussion relating to claim 1, the combination of Abadeer and O'Shaughnessy does not teach or suggest an assembly of switches, connected to turn the series connection into a parallel association of said resistors between *two programming terminals intended to receive a supply voltage*, as recited in claim 10.

Second, the combination of Abadeer and O'Shaughnessy does not teach or suggest an assembly of switches comprising MOS transistors with a number of N-channel transistors greater by one than the number of P-channel transistors, as recited in claim 10. As discussed above, the combination of Abadeer and O'Shaughnessy instead teaches an external self-calibrating RC oscillator circuit.

In view of the foregoing, claim 10 patentably distinguishes over any combination of Abadeer and O'Shaughnessy, thus the rejection under §103 is improper and should be withdrawn. Claims 11-14 depend from claim 10 and are patentable for at least the same reasons.

Claims 15-19:

Claim 15 is directed to a resistive element controllable to irreversibly decrease its value, comprising several polysilicon resistors connected in series between two input/output terminals of the resistive element, an assembly of switches, connected to turn the series connection into a parallel association of said resistors between two programming terminals intended to receive a supply voltage, wherein said switch assembly comprises as many switches as the resistive element comprises resistors, one of said input/output terminals being the same as one of said

programming resistors, and wherein said switches are formed of MOS transistors distributed half and half between P-channel transistors and N-channel transistors.

As should be appreciated from the above discussion relating to claim 10, the combination of Abadeer and O'Shaughnessy does not teach or suggest two programming terminals intended to receive a supply voltage, or switches are formed of MOS transistors distributed half and half between P-channel transistors and N-channel transistors, as recited in claim 15.

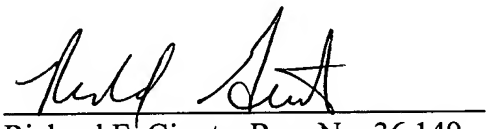
In view of the foregoing, claim 15 patentably distinguishes over any combination of Abadeer and O'Shaughnessy, thus the rejection under §103 is improper and should be withdrawn. Claims 16-19 depend from claim 15 and are patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Michel Bardouillet et al., Applicants

By: 

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